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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,183	01/20/2004	Mie Matsuo	04173.0440	7695

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,183	MATSUO, MIE	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/21/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *1 and 3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4-6, 8, 9, 13-15 and 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino et al (U.S. PG Pub #20020190375), in view of Mikawa et al (U.S. PG Pub #20020115226).

With respect to **claims 2, 5, 8, 14, and 21**, Mashino teaches a semiconductor substrate (Fig. 10, 201), a semiconductor element formation layer (Fig. 10, 202) formed on the semiconductor substrate, and a through plug formed to be partly surrounded by the semiconductor element formation layer and to pass through the semiconductor element formation layer and the semiconductor substrate without being in contact with the formation layer (Fig. 10, 217) as set forth in claim 2; and furthermore teaches a pattern portion formed above the semiconductor element formation layer comprising copper and without being in contact with the through plug (Fig. 10, 205b and Paragraph 117), as set forth in claim 5; and a pattern portion formed above the semiconductor element formation layer comprising copper wherein the through plug is partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 205b and Paragraph 117), as set forth in claim 8; and that the through

plug has a columnar electric conductor made of copper (Paragraph 98) and an insulation layer made of silicon oxide (Fig. 10, 209 and Paragraph 84), as set forth in claim 14.

Mashino does not teach that on the semiconductor element formation layer there is formed a plurality of diffusion layer patterns or an insulation film formed between the plural diffusion layer patterns. Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12), and furthermore that the insulation film is formed to isolate the plural diffusion layer patterns from one another, as set forth in claim 21. It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor element formation layer of Mashino with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the diffusion layer pattern, in order to realize a ferroelectric memory device.

With respect to **claims 7, 4, and 13**, Mashino teaches a semiconductor substrate (Fig. 10, 201), a semiconductor element formation layer (Fig. 10, 202) formed on the semiconductor substrate, a pattern portion formed above the semiconductor element formation layer using copper as a material thereof (Fig. 10, 205b and Paragraph 117), and a through plug formed to be partly surrounded by the semiconductor element formation layer and to pass through the semiconductor element formation layer and the semiconductor substrate without

being in contact with the formation layer (Fig. 10, 217), as set forth in claim 7; and furthermore teaches that a pattern portion formed above the semiconductor element formation layer comprising copper and without being in contact with the through plug (Fig. 10, 205b and Paragraph 117), as set forth in claim 4; and that the through plug has a columnar electric conductor made of copper (Paragraph 98) and an insulation layer made of silicon oxide (Fig. 10, 209 and Paragraph 84), as set forth in claim 13.

Mashino does not teach that on the semiconductor element formation layer there is formed a plurality of diffusion layer patterns or an insulation film formed between the plural diffusion layer patterns to isolate the plural diffusion layer patterns from one another. Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor element formation layer of Mashino with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the insulation film, in order to realize a ferroelectric memory device.

With respect to **claim 9, 6, and 15**, Mashino teaches a plurality of semiconductor chips (Fig. 11, 215), at least one of the plural semiconductor chips including: a semiconductor substrate (Fig. 10, 201), a semiconductor element

formation layer (Fig. 10, 202) formed on the semiconductor substrate, a pattern portion formed above the semiconductor element formation layer using copper as a material thereof (Fig. 10, 205b and Paragraph 117), a through plug formed to be partly surrounded by the semiconductor element formation layer and to pass through the semiconductor element formation layer and the semiconductor substrate without being in contact with the formation layer, the through plug being partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 217) and being insulated from the pattern portion (Fig. 10, 209), and a connecting member electrically connecting the through plugs of the at least one of the plural semiconductor chips to a semiconductor chip of the plural semiconductor chips other than the at least one of the plural semiconductor chips (Fig. 11, 210); and furthermore teaches a pattern portion formed above the semiconductor element formation layer comprising copper and without being in contact with the through plug (Fig. 10, 205b and Paragraph 117), as set forth in claim 6; and that the through plug has a columnar electric conductor made of copper (Paragraph 98) and an insulation layer made of silicon oxide (Fig. 10, 209 and Paragraph 84), as set forth in claim 15.

Mashino does not teach that on the semiconductor element formation layer there is formed a plurality of diffusion layer patterns or an insulation film formed between the plural diffusion layer patterns to isolate the plural diffusion layer patterns from one another. Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation

film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor element formation layer of Mashino with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the insulation film, in order to realize a ferroelectric memory device.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mikawa, further in view of Mayashita et al (U.S. PG Pub #2001045605).

With respect to **claim 10**, Mashino and Mikawa teach all of the limitations of claim 7, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

With respect to **claim 11**, Mashino and Mikawa teach all of the limitations of claim 2, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as

taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

With respect to **claim 12**, Mashino and Mikawa teach all of the limitations of claim 9, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mikawa, in view of Sakao (U.S. Patent #6166425).

With respect to **claims 16 and 19**, Mashino and Mikawa teach all of the limitations of claim 7, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Mashino

based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 17**, Mashino and Mikawa teach all of the limitations of claim 2, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 18**, Mashino and Mikawa teach all of the limitations of claim 9, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance between the diffusion layers be

smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 20**, Mashino and Mikawa teach all of the limitations of claim 9, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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